# Computer Architecture MCQ

4th semester CS/IT
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1) Who developed the basic architecture of computer?
a)Blaise Pascal b) Charles Babbage c) **John Von Neumann** d) None of the above

2) Which of the following is not considered as a peripheral device?
a) **CPU** **b) Keyboard** c) Monitor d) All of the above

3) Which of the following computer memory is fastest?
**a) Register** **b)** Hard disk **c)** RAM **d)** None of the above

4) Which of the following operations is/are performed by the ALU?
a) Data manipulation b) Exponential c) Square root d) **All of the above**

5) Which of the following format is used to store data?
a) Decimal b) Octal c**) BCD** d) Hexadecimal

6) Which of the following memory of the computer is used to speed up the computer processing?
**a) Cache memory** b) RAM c) ROM d) none of the above

8) Computer address bus is -
a) Multidirectional b) Bidirectional c**) Unidirectional** d).None of the above

9) Which of the following circuit is used to store one bit of data?
a) **Flip Flop** b) Decoder c) Encoder d) Register

10) Which of the following is a way in which the components of a computer are connected to each other?
a) Computer parts b) **Computer architecture** c) Computer hardware d) None of the above

11) The address in the main memory is known as –
a) Logical address b) **Physical address** c) Memory address d) None of the above

12) Subtraction in computers is carried out by –

a) 1's complement b**) 2's complement** c) 3's complement d) 9's complement

13) Which of the following memory unit communicates directly with the CPU?
a. Auxiliary memory **b. Main memory** c) Secondary memory d.) None of the above

14) The collection of 8-bits is called as -.
a) **Byte** b) Nibble c) Word d) Record

15) Which of the following is a group of bits that tells the computer to perform a particular operation?
a) Accumulator b) Register c) Instruction code d)None of the above

16) Where is the document temporarily stored during working on a document on PC?
a)ROM b) CPU c) **RAM** d) Flash memory

17) Where is the decoded instruction stored?
a) Registers b) MDR c) PC d) IR

18) The status bit is also called as –
a) **Unsigned bit** b) Signed bit c) Flag bit d.) None of the above

19) Which of the following register can interact with the secondary storage?
a) PC b) **MAR** c) MDR d) IR

20) Which of the following is not considered as a peripheral device?
**a) CPU** **b) Keyboard** c) Monitor d) All of the above

21) Which of the following is an essential data transfer technique?
a) MMA b) **DMA** c) CAD d) CAM

22) RISC stands for –
a) **Reduce Instruction Set Computer** b) Risk Instruction Sequential Compilation
c) Risk Instruction Source Compiler d) None of the above

23) In which of the following term the performance of cache memory is measured?
a) Chat ratio b) Hit **ratio** c) Copy ratio d)Data ratio

24) Which of the following is the function of the control unit in the CPU?
a) It stores program instruction b) It decodes program instruction
c)It performs logic operations d) None of the above

25) Which of the following computer register collects the result of computation?
a) **Accumulator** **b)** Instruction Pointer c) Storage register d) None of the above

26) Which of the following building block can be used to implement any combinational logic circuit?
a) AND b) OR c) **NAND** **d)** None of the above

27) What does a computer bus line consists of?
**a) Set of parallel lines** **b)** Accumulators **c)** Registers d) None of the above

28) Which of the following is performed by half adder?
a)Binary addition operation for 2 decimal inputs
**b) Binary addition operation for 2 binary inputs**
c) Decimal addition operation for 2 decimal inputs
d) Binary addition operation for 2 binary inputs

29) Circuits that can hold their state as long as power is applied is _____
a) Dynamic memory b) Static memory c) Register d) Cache

30) The minimum time delay between two successive memory read operations is _____
a)**Cycle time** b) Latency c) Delay d) None of the mentioned

31) The drawback of building a large memory with DRAM is _____
a) The large cost factor b) The inefficient memory organization
c) The **Slow speed of operation** d) All of the mentioned

32) The fastest data access is provided using _____
a) Caches b) DRAM's c) SRAM's d) **Registers**

33) The next level of memory hierarchy after the L2 cache is _____
a) Secondary storage b) TLB c) Main memory d) **Register**

34) The memory blocks are mapped on to the cache with the help of _____
a) Hash functions b) Vectors c) **Mapping functions** d) None of the mentioned

35) During a write operation if the required block is not present in the cache then _____ occurs.
a) Write latency b) Write hi c) Write delay d) **Write miss**

36)The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____
a) Set associative b) Associative c) **Direct** d) Indirect

37) In _____ protocol the information is directly written into the main memory.
a) **Write through** b) Write back c) Write first d) None of the mentioned

38) The benefit of using this approach is _____
a ) It is cost effective b) It is highly efficient c) It is very reliable d) **It increases the speed of operation**

39) The transfer of large chunks of data with the involvement of the processor is done by _____
a) **DMA controller** b) Arbitrator c) User system programs d) None of the mentioned

40) The unit which acts as an intermediate agent between memory and backing store to reduce process time is _____
a) TLB's b) Registers c) Page tables d) **Cache**

41). The situation wherein the data of operands are not available is called _____
a) **Data hazard** b) Stock c) Deadlock d) Structural hazard

42) The fetch and execution cycles are interleaved with the help of _____
a) Modification in processor architecture **b) Clock** c) Special unit d) Control unit

43) The algorithm which replaces the block which has not been referenced for a while is called _____
a) **LRU** b) ORF c) Direct d) Both LRU and ORF

44) The algorithm which removes the recently used page first is _____
a) LRU b) **MRU** c) OFM d) None of the mentioned

45) In LRU, the referenced blocks counter is set to'0′ and that of the previous blocks are incremented by one and others remain same, in the case of _____
a) **Hit** b) Miss c) Delay d) None of the mentioned

46) In the case of, Zero-address instruction method the operands are stored in _____
a) Registers b) Accumulators c) **Push down stack** d) Cache

47) The addressing mode which makes use of in-direction pointers is _____
a) **Indirect addressing mode** b) Index addressing mode
c) Relative addressing mode d) offset addressing mode

48) The addressing mode/s, which uses the PC instead of a general purpose register is _____
a) Indexed with offset b) **Relative** c) Direct d) Both Indexed with offset and direct

49) The addressing mode, where you directly specify the operand value is _____
a) **Immediate** b) Direct c) Definite d) Relative

50)The effective address of the following instruction is MUL 5(R1,R2).
a) 5+R1+R2 b) 5+(R1*R2) c) **5+[R1]+[R2]** d) 5*([R1]+[R2])

51) In memory-mapped I/O _____
a) **The I/O devices and the memory share the same address space**
b) The I/O devices have a separate address space
c) The memory and I/O devices have an associated address space
d) A part of the memory is specifically set aside for the I/O operation

52) The usual BUS structure used to connect the I/O devices is _____
a) Star BUS structure ` b) Multiple BUS structure
c) **Single BUS structure** d) Node to Node BUS structure

53) The system is notified of a read or write operation by _____
a) Appending an extra bit of the address b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal d) **Sending a special signal along the BUS**

54) The method of accessing the I/O devices by repeatedly checking the status flags is _____
a) **Program-controlled I/** b) Memory-mapped I/O c) I/O mapped d) None of the mentioned

55) The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is?
a) Exceptions b) Signal handling c) **Interrupts** d) DMA

56) The method which offers higher speeds of I/O transfers is _____
a) interrupts b) Memory mapping c) Program-controlled I/O d) **DMA**

57) In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.
a) 24 b) **23** c) 20 d) 16

58) The sign followed by the string of digits is called as _____
a) Significant b) Determinant c) **Mantissa** d) Exponent

59)If the decimal point is placed to the right of the first significant digit, then the number is called _____
a) Orthogonal b) **Normalized** c) Determinate d) None of the mentioned

60) In double precision format, the size of the mantissa is _____
a) 32 bit b) **52 bit** c) 64 bit d) 72 bit

61) We make use of _____ circuits to implement multiplication.
a) Flip flops b) Combinatorial c) **Fast adders** d) None of the mentioned

62) The multiplier is stored in _____
a) PC Register b) **Shift register** c) Cache d) None of the mentioned

63) The _____ is used to coordinate the operation of the multiplier.
a) Controller b) Coordinator c) **Control sequencer** d) None of the mentioned

64)The multiplicand and the control signals are passed through to the n-bit adder via _____
a) **MUX** b) DEMUX c) Encoder d) Decoder
The bits 1 & 1 are recorded as _____ in bit-pair recording.
a) -1 b) 0 c) +1 d) **both -1 and 0**

65) CSA stands for?
a) **Computer Speed Addition** b) Carry Save Addition
c) Computer Service Architecture d) None of the mentioned

66) The computer architecture aimed at reducing the time of execution of instructions is _____
a) CISC b) **RISC** c) ISA d) ANNA

67) Both the CISC and RISC architectures have been developed to reduce the _____
a) Cost b) Time delay c) **Semantic gap** d) All of the mentioned

68) Which of the architecture is power efficient?
a) CISC b) **RISC** c) ISA d) IANA

69) The ROM chips are mainly used to store _____
a) System files b) Root directories c) **Boot files** d) Driver files

70) The disadvantage of the EPROM chip is _____
a) The high cost factor b) The low efficiency
c) The low speed of operation d) **The need to remove the chip physically to reprogram it**

71) In micro-programmed approach, the signals are generated by _____
a) **Machine instructions** b) System programs c) Utility tools d) None of the mentioned

72) A sequence of control words corresponding to a control sequence is called _____
a) **Micro routine** b) Micro function c) Micro procedure d) None of the mentioned

73) Individual control words of the micro routine are called as _____
a) Micro task b) Micro operation c) **Micro instruction** d) Micro command

74) Every time a new instruction is loaded into IR the output of _____ is loaded into UPC.
a) **Starting address generator** b) Loader c) Linker d) Clock

75) The special memory used to store the micro routines of a computer is _____
a) Control table b) **Control store** c) Control mart d) Control shop

76) The small extremely fast RAM is called as _____
a) **Cache** b) Heaps c) Accumulators d) Stacks

77) To organize large memory chips we make use of _____
a) Integrated chips b) Upgraded hardware c) **Memory modules** d) None of the mentioned

78) The chip can be disabled or cut off from an external connection using _____
a) **Chip select** b) LOCK c) ACPT d) RESET

79) The periods of time when the unit is idle is called as _____
a) Stalls b) Bubbles c) Hazards d) **Both Stalls and Bubbles**

80) The contention for the usage of a hardware device is called _____
a) **Structural hazard** b) Stalk c) Deadlock d) None of the mentioned

81) The stalling of the processor due to the unavailability of the instructions is called as _____
a) **Control hazard** b) structural hazard c) Input hazard d) None of the mentioned

82) When using the Big Endian assignment to store a number, the sign bit of the number is stored in _____
a) **The higher order byte of the word** b) The lower order byte of the word
c) Can't say d) None of the mentioned

83) To get the physical address from the logical address generated by CPU we use _____
a) MAR b) **MMU** c) Overlays d) TLB

84) The smallest entity of memory is called _____
a) **Cell** b) Block c) Instance d) Unit

85) The collection of the above mentioned entities where data is stored is called _____
a) Block b) Set c**) Word** d) Byte

86) The type of memory assignment used in Intel processors is _____
a) **Little Endian** b) Big Endian c) Medium Endian d) None of the mentioned

87) RTN stands for _____
a) **Register Transfer Notation** b) Register Transmission Notation
c) Regular Transmission Notation d) Regular Transfer Notation

88) The two phases of executing an instruction are _____
a) Instruction decoding and storage
b) **Instruction fetch and instruction execution**
c) Instruction execution and storage
d) Instruction fetch and Instruction processing

89) When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____
a) **Branch target** b) Loop target c) Forward target d) Jump instruction

90) The condition flag Z is set to 1 to indicate _____
a) The operation has resulted in an error b) The operation requires an interrupt call
c) **The result is zero** d) There is no empty register available

91) The stack frame for each subroutine is present in _____
a) Main memory b) System Heap c) **Processor Stack** d) None of the mentioned

92) The main virtue for using single Bus structure is _____
a) Fast data transfers
b) Cost effective connectivity and speed
c) **Cost effective connectivity and ease of attaching peripheral devices**
d) None of the mention

93) _____ are used to overcome the difference in data transfer speeds of various devices.
a) Speed enhancing circuitory b) Bridge circuits c) Multiple Buses d) **Buffer registers**

94) The bus used to connect the monitor to the CPU is _____
a) PCI bus b) **SCSI bus** c) Memory bus d) Rambus

95) In multiple Bus organization, the registers are collectively placed and referred as _____
a) Set registers b) **Register file** c) Register Block d) Map registers

96) The main advantage of multiple bus organization over a single bus is _____
a**) Reduction in the number of cycles for execution** b) Increase in size of the registers
c) Better Connectivity d) None of the mentioned

97) Write through technique is used in which memory for updating the data
a) Virtual Memory b) Auxiliary memory c) Main memory d) **Cache memory**

98) The main memory in a personal computer is made of
a) Static RAM b) Both **c and d** c) Cache memory d) Dynamic RAM

99) The operation executed on data stored in registers is called
a) **Micro operation** b) Bit operation c) macro operation d) Byte operation

100) The time interval between adjacent bits is called the
a) Word time b) Turnaround time c) **Bit time** d) slice time